



Report on DTE(Adder & Subtractor) Guest Lecture

Title: Report on DTE(Adder & Subtractor) Guest Lecture

Date: 05th August, 2025

Time: 1:00 pm to 03:00 pm

Venue: Classroom 201

Participants: **Second Year Students (CO) from SIOT.**

A guest lecture on the topic “**Digital Technique: Adder and Subtractor**” was successfully conducted on 05th August 2025 at Classroom 201, aimed at enhancing the theoretical and practical understanding of digital circuits among the second-year Computer Engineering students of Saraswati Institute of Technology (SIOT).

The session was conducted from 1:00 PM to focusing on the fundamentals and applications of binary addition and subtraction, including both combinational and sequential circuit implementations. The guest speaker explained various types of adders and subtractors such as half adder, full adder, half subtractor, full subtractor, and also provided insights into carry look-ahead adders and their role in speeding up digital systems.

The lecture was interactive and engaging, encouraging students to ask questions and participate in discussions. Real-world examples and circuit demonstrations were shared to strengthen conceptual clarity. The session concluded with a Q&A segment and positive feedback from students, who appreciated the practical relevance of the lecture in relation to their academic curriculum.

Overall, the guest lecture was highly informative and contributed significantly to students' understanding of essential digital techniques in computing systems.



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