ASSIGNMENT

Name of subject: DIGITAL TECHNIQUES

Subject Code: 17333

Semester: III

ASSIGNMENT 1:

Introduction to Digital Techniques (16 marks)

3 marks

1) Which are the advantages of digital circuits?

2) convert the following hexadecimal number into binary: (AFB2)16

3) Explain the following terms noise margin, power dissipation, propagation delay

4) Explain fan-out, fan-in and figures of merit

5) convert the following binary number to decimal number: (1011.01)2

6) Perform (9)10-(4)10 using 1's complement method

4 marks

7) Perform the following subtraction using 2's complement method:

(11010)2 - (10000)2

8) Write down the characteristics of CMOS.

9) Perform BCD addition for the

following: i) (85)10 + (39)10 or

ii) (368)10 + (427)10

ASSIGNMENT 2:

Logic gates and Boolean algebra (18 marks)

3 marks

1) Write down any six Boolean laws.

2) Explain principle of duality theorem.

4 marks

3) Prove the following logic expression using Boolean algebra:
i)(A+B)(A+C)=A+BC

ii) A+AB=A+B

4) Write down the truth table, logic symbol and Boolean expression for AND gate using 3 inputs.

5) Write down the truth table, logic symbol and Boolean expression for EX-OR gate using 2 inputs.

ii) Y=AD+BCD+BCD

6) Draw the equivalent circuit of the following gates using NAND gates

i) OR ii) AND

7) Draw logic circuit using universal gates for following logic equation:

Y =ABC+AC+BC

8) Explain EX-OR Gate and EX-NOR Gate.

9) Simplify given expression and draw circuit diagram using only NOR Gate.

Y=ABC +BC+ABC + ABC

10) Prove that

(A+B+C) (A+B+C) (A+B+C)(A+B+C) =A

ASSIGNMENT 3:

Combinational logic circuit. (26 Marks)

Mark 3:

1) Simplify Boolean expression.

$Y = \sum m (2, 4, 6)$

2) Drawhalf adder circuit using k map and realize it by using basic gates.

Mark 4:

3) Draw full adder circuit using k map and realize it by using basic gates.

4) Draw 4:1 mux. And give its truth table.

5) Implement 16:1 Mux using 4:1 Mux.

6) Implement the following expression using multiplexer $Y=\sum m (0, 1, 2, 3, 6, 7)$.

7) What is K-map?

8) Design 4:1 MUX using 2:1 MUX **10 marks:**

9) Explain Half Subtractor with logic implementation of gates.

10) convert the expression Y=AB+AC+BC into the canonical SOP form.

11) Simplify the following three variable Boolean expressions: $Y=\sum m (2, 4, 6)$

12) Implement the following function using 8:1 MUX
$Y=\sum m(0,1,3,4,7)$.

ASSIGNMENT 4:

Sequential logic circuit (28 marks)

3 marks:

1. Explain J-K Flip Flop.

2. Explain 1-bit memory cell with working.

3. Draw the neat diagram of Master Slave J-K Flip Flop .

4 marks:

4. Draw the logical circuit diagram of clocked S-R Flip Flop using NAND gates.

   Description working.

5. Explain Race Around condition in J-K Flip Flop.

6. Draw the Block Diagram of sequential logic circuit and state the

   importance of clock signal.

7. Explain the triggering methods of Flip Flop.

8.Draw the neat diagram of Master Slave J-K FlipFlop .

9.Design clocked S-R Flip Flop with Preset and Clear.

10.Explain the significance of Preset and Clear in JK Flip Flop.

ASSIGNMENT 5:

A-D and D-A Converter (12 marks)

3 marks:

1. Give two Advantages and Dis-Advantages of ADC.
2. Compare Weighted Register DAC and R2R Ladder type DAC. 3.List any 4 applications of AD converter.
3. 4.An 8 bit ADC has maximum voltage of 15V.What voltage change would each bit represent?
4. Classify the memories. What are the mechanism used for erasing EPROM?
5. Draw the Circuit Diagram of R-2R Ladder method of DAC.
6. Draw the block Diagram of Successive Approximation method of ADC.
7. Explain the Specifications of DAC.
8. Explain any 4 specifications of ADC.